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Comparison of Conditional Internal Activity Techniques for Low Power Consumption and High Performance Flip-Flops

Jyoti[1], Dr. Malay Ranjan Tripathy[2] and Vijeta[3]

***Abstract*– This paper reviews the three Conditional internal activity Techniques for high performance flip-flops namely Conditional Capture, Conditional Precharge and Conditional Discharge techniques. These techniques are reviewed in terms of power and delay and classified based on how to prevent or reduce the internal switching activity. Application of the Conditional techniques results in improvement of Energy-Delay product and saving of power consumption for quiet input. Low power flip-flops are vital for the design of low-power digital systems. In this paper low power high performance flip flops are reviewed based on these techniques .Comparison summary of recent results of flip-flop characteristics based on these techniques is also specified.**

***Index Terms*– Digital CMOS, Flip-Flop, Latches, Low Power, Very Large Scale Integration (VLSI)**

I. INTRODUCTION

POWER consumption in high-performance integrated circuits has been one of the most serious limitations in high-performance designs recently. Power optimization techniques are applied in different levels of digital design. In order to optimize the power dissipation of digital systems low-power methodology should be applied throughout the design process. VLSI designers have used speed of the circuit as the performance metric. Two conflicting constraints in this field are high performance and small area. But now a day's power dissipation is becoming an important in a design. Low power design is a new era in VLSI technology.

Low power design is used for portable applications such as wristwatches and pacemakers as well as to reduce the power of high performance systems. Systems with high clock frequency are emerging with improved operation speed and large integration density.

Low power design basically deals with power estimation, its analysis and power minimization [1]. The clock system consists of the clock interconnection network, flip-flops and latches. These components are one of the most power consuming components in a very large scale integration (VLSI) system. It accounts for 35%–60% of the total power dissipation [2]. Reducing the power consumed by flip-flops will have a profound impact on the total power consumption. In terms of timing perception, flip-flop latency consumes a large portion of the cycle time whereas the operating frequency increases. Consequently flip-flop choice and design has a intense effect in reducing the power dissipation in high-performance systems. These reasons are the main driving force for the increased importance in flip-flop design and analysis. A wide selection of different flip-flops can be found in the literature [1]–[18]. Latches and flip-flops have a straight impact on power consumption and speed of VLSI systems. For that reason study on low-power latches and flip-flops is unavoidable.

A common flip-flop with the best performance, lowest power consumption, and maximum robustness against noise would be an ideal component to be included in cell libraries. Increasing the performance of flip-flops involves considerable power and robustness trade-offs. So, a set of different latches and flip-flops with different performances are necessary to bind the use of more power consuming and noise-sensitive elements only for smaller portion of the chips with performance-critical units. This eliminates avoidable increase in power consumption as well as robustness degradations, which would result in overall decrease in noise margin requiring extra careful design.

All the hard edge triggered flip-flops for example master-slave flip-flops and sense amplifier flip-flops are characterized by positive setup time and causes large input to output delay. On the other hand, pulse-triggered flip-flops reduce the two stages into single stage. These flip-flops are characterized by the soft edge property and due to this reason logic complexity is reduced leading to small input to output delays. Pulse triggered flip-flops are better than hard edge flip-flop because they have negative setup time. Pulse-triggered flip-flops can be divided into two type's namely implicit and explicit flip-flops. In implicit-pulse triggered flip-flops pulse is generated inside the flip-flop. Hybrid latch flip-flip (HLFF), semi-dynamic flip-flop (SDFF), and implicit-pulsed data-close-to-output flip-flop (ip-DCO) are implicit-pulse triggered flip-flops.

Whereas in explicit-pulse triggered flip-flops, the pulse is generated externally, for example, explicit-pulsed data-close-to-output flip-flop. Explicit-pulse triggered flip-flops consume more energy but it has several advantages. Double-edge triggering is easy to implement in ep-FF, but it is difficult to

[1]Research Scholar, Department of Electronics and Communication Engineering, Singhania University, Pacheri Bari, Jhunjhunu, Raj., India
Email: jyotikohar@gmail.com
[2]Professor, Department of Electronics and Communication Engineering, Amity School of Engineering and Technology, Noida, Uttar Pradesh, India
[3]Department of Electronics and Communication Engineering, Banglore Institute of Technology, Banglore, India

implement in ip-FF and ep-FF have the advantage of better performance as the height of the nMOS stack in ep-FF is less than that in ip-FF.

This paper is organized as follows. Section 2 describes different Conditional Techniques for low power and high performance design which are used to reduce the switching activity inside flip-flops. Section 3 presents some low power flip-flops and Section 4 describes Comparison of Flip-Flop characteristics. Section 5 concludes this paper.

II. CONDITIONAL TECHNIQUES

One effective technique to obtain power saving in case of flip-flops is based on the utilization of dynamic structure. Lots of power is wasted in flip-flops which are using dynamic behavior due to the internal switching activity. By reducing the unnecessary switching activities, we can reduce the overall power dissipation. So to reduce the internal switching activities, we can use two techniques namely Conditional precharge technique and Conditional capture technique.

Conditional capture flip-flop has been developed to reduce the power consumption in internal nodes of a no. of high performance flip-flops. Major advantage of CCFF is that there is no speed penalty. Setup time of CCFF is increased in comparison to Hybrid Latch Flip-Flop(HLFF).There are two main reason behind it. First is the large recovery time on the node Q and second is increase in sampling time for capturing input 'Low'. Many additional transistors are needed in Condition capture technique for some flip-flops like Semi-Dynamic Flip-flop (SDFF).Conditional Precharge Flip-Flop (CPFF) was proposed by Nedovic.

In this technique internal node precharging is determined by the output signal. CPFF has large setup time similar to CCFF. To solve this problem improved version of CPFF was introduced without consumption cost. A new technique Conditional discharge technique is also used for the same purpose. This technique will overcome the limitations of the techniques discussed above. This paper reviews all these three Conditional techniques. In literature many techniques are discussed [40]-[45].

According to the requirements of the system, the designer has to consider all the parameters while choosing a structure for flip-flops. Factors which are advantageous in flip-flops are as follows [36]-[39]:

1. High speed
2. Low power consumption
3. Small area
4. Less number of transistors
5. Supply voltage scalability
6. Low glitch probability
7. Insensitivity to clock edge
8. Insensitivity to process variables
9. Less internal activity when data activity is low

Trade-offs between desired parameters, make this decision a multi-dimensional optimization problem for high-performance systems. A multi-dimensional Optimization problem for a non-linear system that usually has hundreds of variables is unfortunately impossible to solve within the limited design time. This will give us a good understanding of different structures and make the decisions easier for the designers.

A. Conditional Precharge Technique

Conditional precharge technique has been applied to low clock-swing flip-flop and save both clock system power and supply power.In this technique the discharging path is controlled to avoid the precharging of the internal node when the input remains high as shown in fig 1 which depicts the general scheme of Conditional precharge technique.

There are number of flip-flops techniques with internal activity gated upon the actual requirement to carry out signal transition. These conditional techniques based on clock pulse generation [13].

The flip-flop's output is checked and the transition is allowed only if it is used to change the value of output. The choice of flip flop and its design has a profound effect in decreasing the power dissipation. Pulse triggered flip-flops are better than master slave flip-flops in performance due to timing issues.

The components of sequential circuit in a CMOS circuit are considered as major factors to the power dissipation since one of the inputs in it of certain component is the clock which is the only signal that switches all the time. According to the recent studies, clock signal in digitals computers consume a large percentage (15%-45%) of the system power.

So by reducing the power dissipation, we can reduce the power dissipation to a greater extent in digital VLSI circuits. This goal can be achieved by two means. Firstly by eliminating the waste power dissipation caused by switching the clock in non triggering direction. Secondly, to block the clock signal feeding into the flip-flops during their holding states so as to reduce the power dissipation. To reduce the power consumption in flip-flops Conditional capture, clock-on-demand, data transition look-ahead techniques have been developed.

To short out these charging and discharging activities a simple pmos transistor is used in the precharging path.This flip-flop cause higher setup time for high-to-low transition. A no. of flip-flops used this technique. For example, CPFF [13], DE-CPFF [14] and CP-SAFF [15].

The controlling signal is the output Q in case of CPFF and dual edge clocking conditional precharge flip-flop (DE-CPFF) and in CP-SAFF, the control signal is the input D.

B. Conditional Capture Technique

This technique is very attractive in terms of high performance VLSI implementation. Conditional Capture technique eliminates unnecessary transitions to minimize the power without effecting speed. The purpose of Conditional Capture technique is that to derive the internal nodes

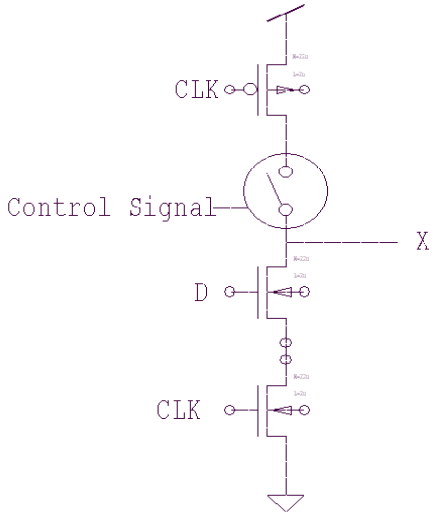

Fig. 1. Conditional precharge technique

significant portion of the power is consumed and the output remains the same. By disabling the redundant internal transtion, it is possible to achieve significant power reduction. Two types of Conditional Capture technique have been discussed in [16] namely single ended and differential implementation.

The main disadvantages of this technique are related to increase in setup time for zero sampling time. So setup time is the limiting performance parameter. Conditional Capture technique is totally based on clock gating idea. This technique is shown in fig 2. Conditional Capture technique is mostly used for implicit pulse triggered flip-flop, for example CCFF. In this flip-flop, a transparency window is used for the sampling of the input. Transparency window is determined by the time when both transistors are on at the same time. The output depend on the input means output Q will be high when input is high. Clock gating in the Conditional Capture technique results in redundant power consumption. Conditional Precharge technique is better than Conditional Capture technique in terms of Energy-Delay-Product (EDP) means it reduce the EDP. But Conditional Precharge technique can only be applied to ip-FF.

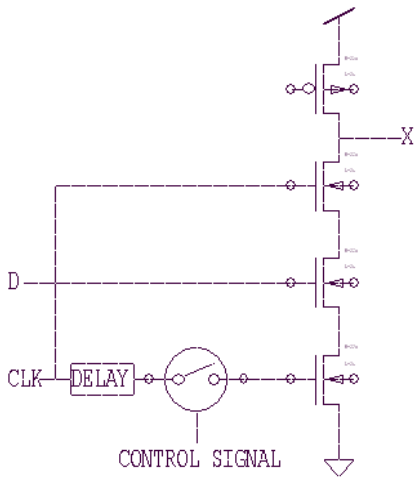

Fig. 2. Conditional capture technique

C. Conditional Discharge Technique

Power saving approach, clock-gating used in Conditional Capture Technique results in redundant power consumed by the gate controlling the delivery of the delayed clock to the flip-flop and Conditional Precharge Technique can only be applied to implicit flip-flop. So to overcome these limitations of these techniques, a new technique, Conditional Discharge Technique is used. This technique can be used for both implicit as well as explicit pulse triggered flip-flops.This technique has been already used by a novel implicit pulsed level convert flip-flop to reduce the overhead incurred with level conversion flip-flops(LCFF).To further decrease the power consumption,Double –edge triggering is also used.In terms of power ,DE-LCFF dissipiates about 18% less power than SLLS and 20% less power than SPFF.DE-LCFF has better PDP.The clocked-pseudo-NMOS(CPN) level conversion flip-flop combine the Conditional Discharge technique and pseudo-NMOS technique.This new CPN-LCFF outperform previous flip-flop in terms of power and delay.

This technique is also used to present a new flip-flop Conditional Discharge flip-flop. Conditional Discharge Technique controlled the discharge path, when input is stable (High) and eliminate the extra switching activity. CDFF use a pulse generator which is suitable for double edge sampling.CDFF has two stages. First is responsible for capturing the Low-to-High transition and second stage captures the High-to-Low input transition. CDFF features less switching noise generation which is very important issue in mixed signal circuits.

III. LOW POWER FLIP FLOP

Flip-flop choice and design has a deep effect both in reducing the power dissipation and in providing more slack time in high-performance systems. Pulse triggered flip-flop

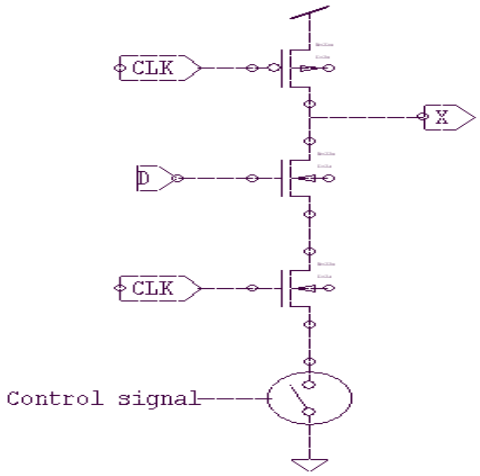

Fig. 3. Conditional Discharge technique

are of two types namely implicit and explicit pulse triggered flip flop. This classification is depending on the pulse generators they use. In implicit-pulse triggered flip-flops the pulse is generated inside the flip-flop. Example of this is hybrid latch flip-flip (HLFF),semi-dynamic flip-flop (SDFF).In explicit-pulse triggered flip-flops (ep-FF), the pulse is generated externally and example for this is explicit-pulsed data-close-to-output flip-flop (ep-DCO). Ep-FF consumes more energy due to the explicit pulse generator.

A. Semi-Dynamic Flip-Flop

Semi-Dynamic Flip-Flop [34] is a high performance flip-flop because of its small delay and simple topology. It is measured to be one of fastest flip-flops today. SDFF is not suitable for applications where low power is required since its power consumption limits its use. Better performance of this circuit is targeted by use of precharging technique on internal node and eliminating low-to-high transitions from critical path, ending with only one transistor path at the output structure of the flip-flop allows logic to be collapsed into flip-flop circuit with very small penalty in number of transistors and performance .It considerably reducing both critical paths in the system and the chip area. It has been noticed that significant portion of power dissipated in SDFF occurs due to avoidable and false transitions that result in glitches usually increasing the power consumed by successive logic as well.

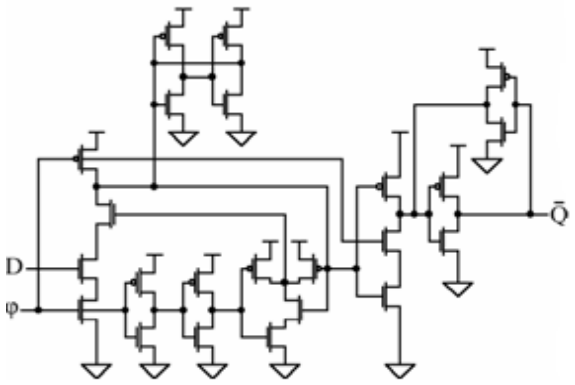

Fig. 4.Semi-Dynamic Flip-Flop [34]

B. Hybrid Latch Flip-Flop

Hybrid latch flip flop is one of the high performance flip flop. It generate the explicit transparency window which allow the transition and due to this property this flip flop results in small delay and small area but small power consumption is there. Principle of operation is explained by three stages.

First stage generates the glitch conditionally in the transparency window. Second stage captures the generated glitch. Every time when the input is high the glitch is generated, regardless of previous state of output. Circuit is shown in Fig. 4.

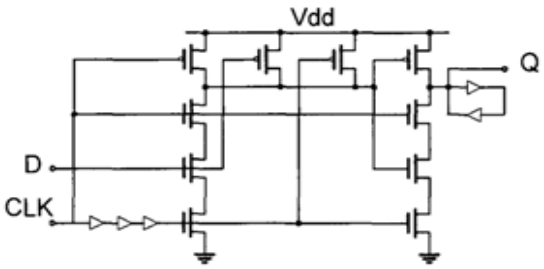

Fig. 5. Hybrid Latch Flip-Flop [13]

It has some disadvantages as well: in order to change the state of HLFF, the keeper has to be overpowered, which introduce another portion of unnecessary power consumption and which causes increase in the delay. Due to this HLFF is not suitable for applications where low power is required since its power ion limits its utilization.

C. Explicit- Pulsed Data-Close-To-Output Flip-Flop

Fig. 6 and Fig. 7 illustrate the diagram of the Explicit-Pulse Data-Close-to-Output flip-flop (ep-DCO). It is measured as one of the fastest flip-flops due to its semi-dynamic nature [10]. Fig. 6 is the Dual-pulse generation circuit of the Explicit-Pulse Data-Close-to-Output flip-flop. It uses the delay of three inverters to generate the pulse at clock. In this flip-flop, there are two stages, the first stage is dynamic and the second stage is static in nature. It consists of six transistors-M1, M2, M3, M4, M5 and M6. The input data is connected to M2 transistor. When the flip-flop is in transparent period, the input data propagates to the output after this period M3 and M5 will turn off due to low voltage. When the point X transform to the high voltage, So M4 is off and M1 is on after the transparent period. There are some disadvantages of Explicit-Pulse Data-Close-to-Output flip-flop. There is lot of power consumption at the internal node X and due to the frequent charging and discharging of node X in each clock cycle causes glitches to appear at the output. These glitches propagate increase the switching power consumption but also cause the noise problems that may cause the system out of order [35].

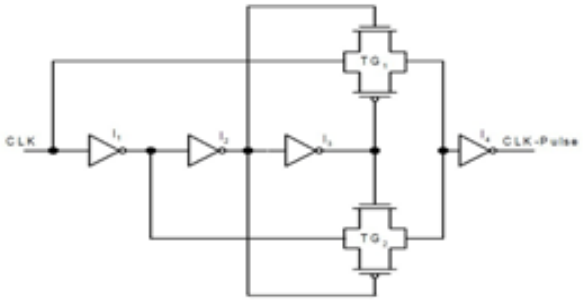

Fig. 6. Dual-pulse generation circuit [10]

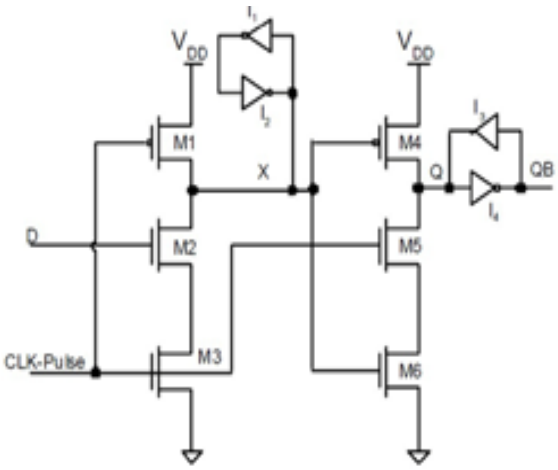

Fig.7. Explicit- Pulsed Data-Close-To-Output Flip Flop [10]

IV. COMPARISON OF CONDITIONAL TECHNIQUE BASED FLIP-FLOP CHARACTERISTICS

Table 1 shows the simulation results of various flip-flops. In terms of delay, CDFF and ep-DCO have the smallest delay because ep-DCO has less nMOS stack height and CDFF uses dual path which generally has better driving ability to help achieve small delay and in terms of the power consumption, CDFF consumes minimum power whereas ep-DCO and imCCFF consume more power because of redundant switching activity. In analysis of PDP comparison, CDFF has the smallest PDP.

V. CONCLUSION

Power estimation and optimization are needed to formulate a low power design, which is required for current and future VLSI design. Different types of flip-flops are studied in this paper for low power applications. In this paper conditional internal activity flip-flop techniques are reviewed. A new technique, Conditional discharge is also reviewed. It reduces the switching activity of some internal nodes in flip-flop. This technique is applied to new flip-flop named CDFF. The Conditional Discharge Technique could be applied to implicit pulsed flip-flops like ip-DCO and HLFF. Comparison of some Conditional Technique based Flip-Flop Characteristics is also summed up. Conditional Techniques are suitable for the application in the high performance VLSI circuits in future.

TABLE 1
FLIP-FLOP CHARACTERISTICS COMPARISION IN TERMS OF DELAY, POWER, AND POWER DELAY PRODUCT

	DQ(ps)	P(uW)	PDP(fJ)
CCFF	206	22.6	4.66
imCCFF	233	27	6.29
CPFF	189.2	22.4	4.24
DE-CPFF	226	21.6	4.88
CDFF	185	20.2	3.74
ep-DCO FF	184	24.4	4.49

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